Hardware Interlock System of the Hall B Silicon Vertex Tracker

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The Hardware Interlock System for the Hall B Silicon Vertex Tracker (SVT) is a standalone, backup system designed to protect the SVT from damage in the event the EPICS-based slow controls system fails, or if network communication is lost.

The Hardware Interlock System is a reconfigurable, embedded controller, and acquisition system, based on National Instruments' CompactRIO Programmable Automation Controller (PAC) platform. The hardware architecture includes I/O modules, a reconfigurable FPGA, and an integrated dual-core controller, which runs on a LabVIEW Real Time Linux operating system. The system does not rely on network communications and is independent of the EPICS-based slow control system.

The CompactRIO of the Hardware Interlock System obtains all monitored signals from the SVT patch panel, Fig. 1. Table I shows the type and number of signals monitored, and the output interfaces to the Mpod's HV/LV crates and chiller.

Corrective action is taken if a signal is outside pre-set limits (fault conditions). Under fault conditions, the system disables the Mpods via the front panel connector on the Mpod controller; once disabled, EPICS controls are overridden and all channels of the Mpod crate will ramp down at their pre-programmed rate. A reset of both the Hardware Interlock System and the EPICS slow controls system of the Mpod controller is needed to re-power the channels.

Additionally, the Hardware Interlock System will disable the SVT chiller, by sending a signal to the BiRa Systems Model 8880-1B1Y AC Power Module from which the AC power to the chiller is supplied. To detect condensation, a water sensor, which uses the capillarity effect of liquid, and a Panasonic light emitter and receiver, is used. A controller unit provides power to the water sensor and an interface to the PAC. Such a condensation/leak detection system is required for coolants that have low conductivity because typically-used resistive-based water sensors will not work. Upon detection of condensation, the chiller is shut down, along with the Mpod channels.

The user interface of the Hardware Interlock System allows the operator to remotely monitor the SVT, to set interlock trip levels, and to reset the system after an interlock trip. The Hardware Interlock System does not require the user interface program to be running to protect the SVT because it is running locally on the dual-core controller.

For safety, only one user interface session is allowed at a time. Figure 2 shows the main screen of the user interface. Figure 3 shows the interlock and "enable setting" screen. Figure 4 shows the installed Hardware Interlock System chassis with the front panel removed.

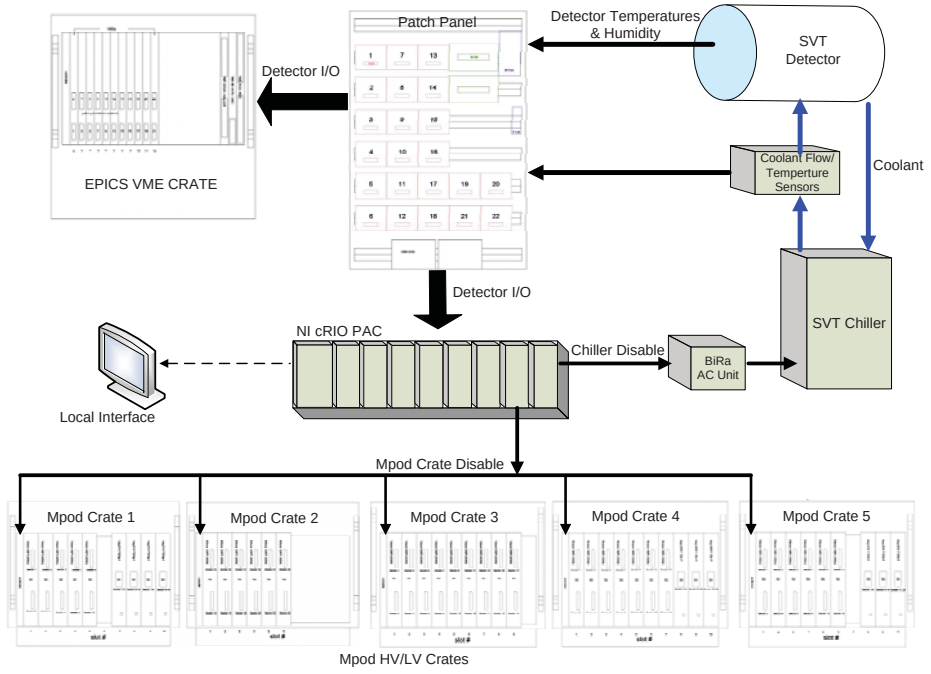

FIG. 1. Block diagram of the Hardware Interlock System.

Signal	# of channels	Input/output	Description
HFCB temperature	4	analog inputs	Monitors top side of a subset of modules in R1, R2, R3, R4
Temperature inside barrel	3	RTD inputs	RTDs are mounted in the support rings; Hardware Interlock System uses the backup sensors
Humidity/dew point inside barrel	3	analog inputs	Humidity sensors are mounted in the support rings; Hardware Interlock System uses the extra sensors
Ambient temperature	2	RTD inputs	RTDs are mounted externally to the detector
Ambient humidity/ dew point	2	analog inputs	Humidity sensors are mounted externally to the detector
Coolant flow	2	analog inputs	Measures coolant flow (external from chiller) (R1–3) + (R4)
Coolant temperature	1	analog input	Measures coolant temperature (external from chiller)
Coolant leak detection	1	analog input	Checks for coolant leaks via sensor mounted in drip pan
Chiller disable	1	analog output	Signal to BiRa AC Unit; removes 120 VAC from chiller
Mpod HV/LV crate disable	5	TTL outputs	Signals to Mpod crate controllers to ramp down low voltage and high voltage

TABLE I. Signals monitored by the Hardware Interlock System.

Since the Hardware Interlock System is the backup system, trip levels for the system are beyond the bounds of the EPICS trip levels. Hence, the EPICS slow controls system (if working correctly) should trip first. If the EPICS slow controls system works correctly, the Hardware Interlock System will never need to take corrective action to protect the SVT.

To conclude, the Hardware Interlock System was installed in August 2015 and has worked continuously and flawlessly since. When the chiller failed in November 2015, the Hardware Interlock System protected the detector by ramping down the HV and LV power supplies.

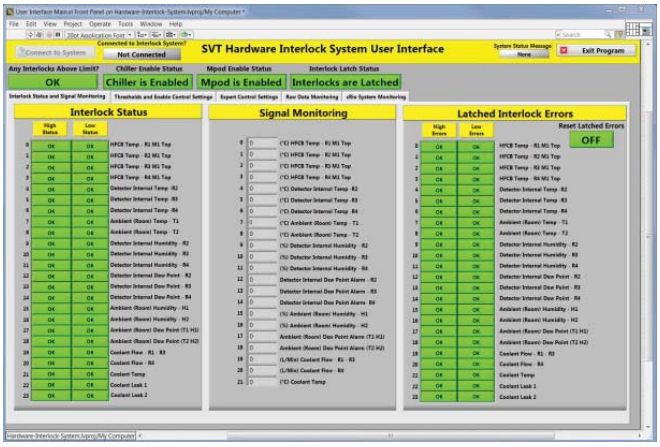

FIG. 2. User interface main screen.

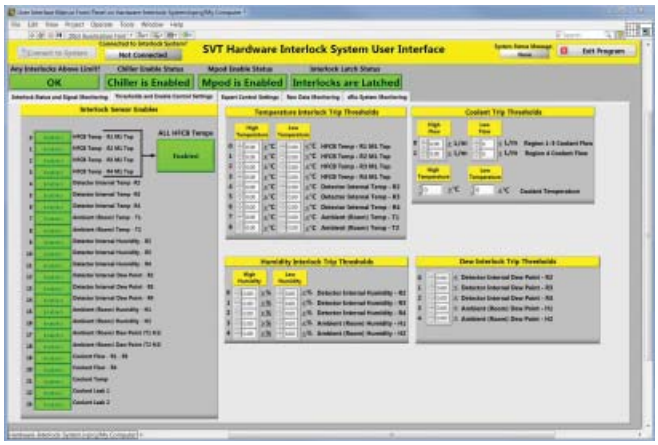

FIG. 3. Interlock and enable settings screen.

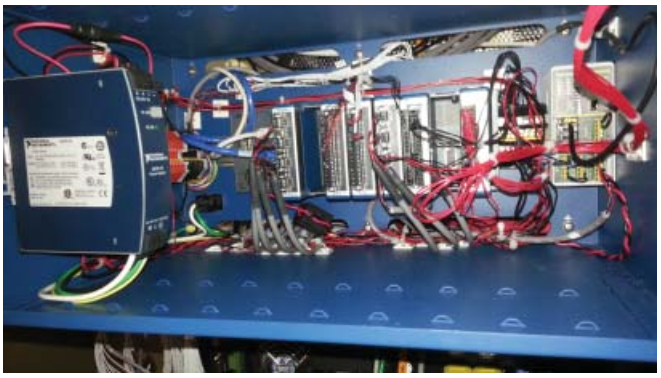

FIG. 4. Inside of installed Hardware Interlock System crate.